

FIG. 1

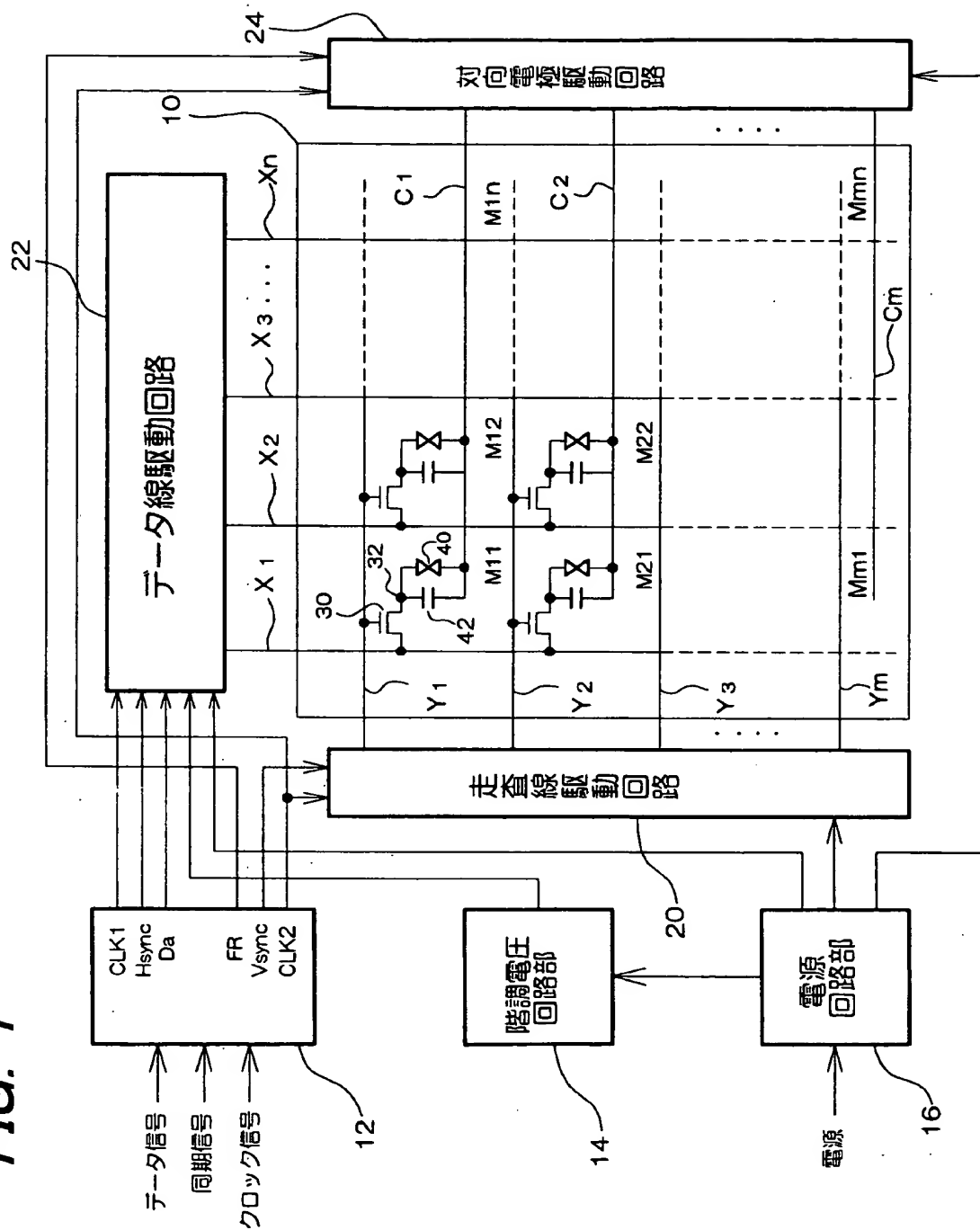


FIG. 2 is a block diagram of a circuit 100. The circuit 100 includes a plurality of flip-flops (FF1, FF2, FF3, FF4, FF5, ..., FF240) and a plurality of comparators (C1, C2, C3, C4, C5, ..., C240). The flip-flops are connected to the comparators. The circuit 100 is powered by a power source (電源) and a clock signal (FR CLK2).

FIG. 2

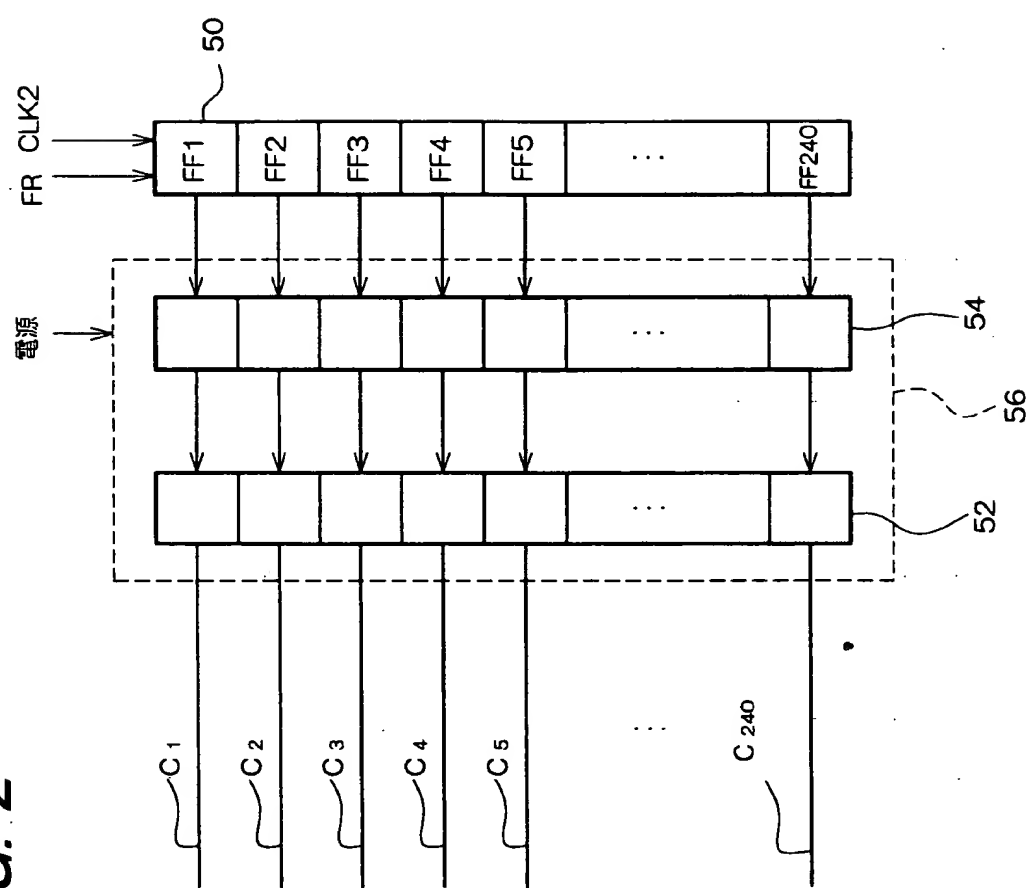
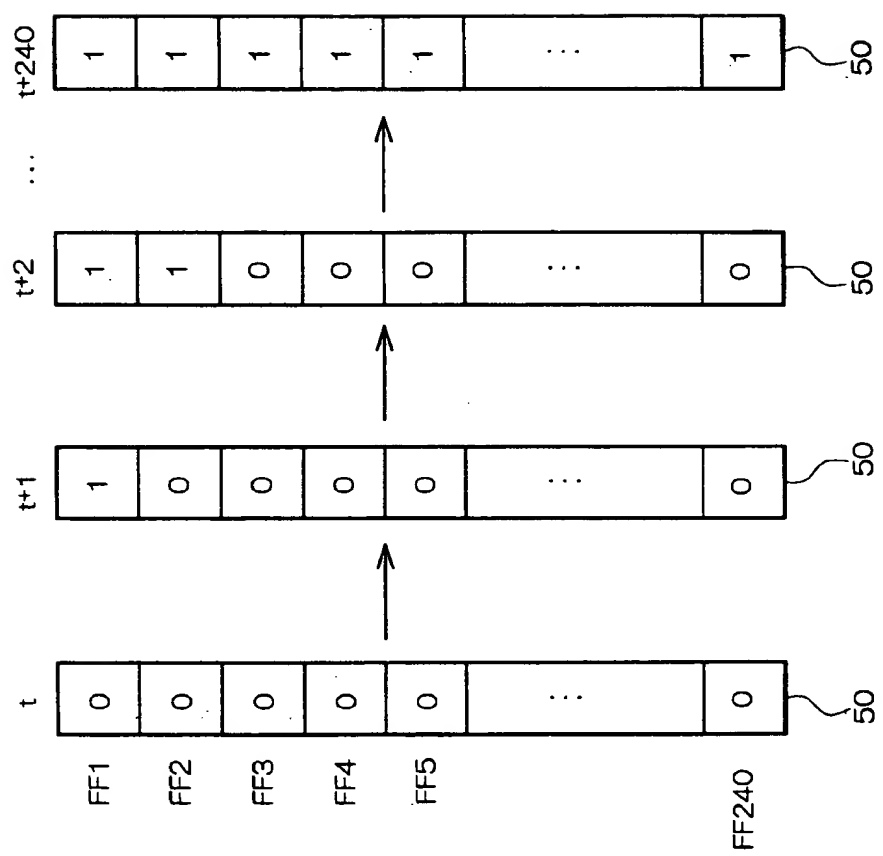


FIG. 3 is a diagram illustrating a sequence of operations over time. The diagram shows four horizontal rows of data, each representing a state at a specific time:  $t$ ,  $t+1$ ,  $t+2$ , and  $t+240$ . Each row is divided into segments, with the first five segments labeled FF1, FF2, FF3, FF4, and FF5, and the last segment labeled FF240. The data values in these segments are as follows:

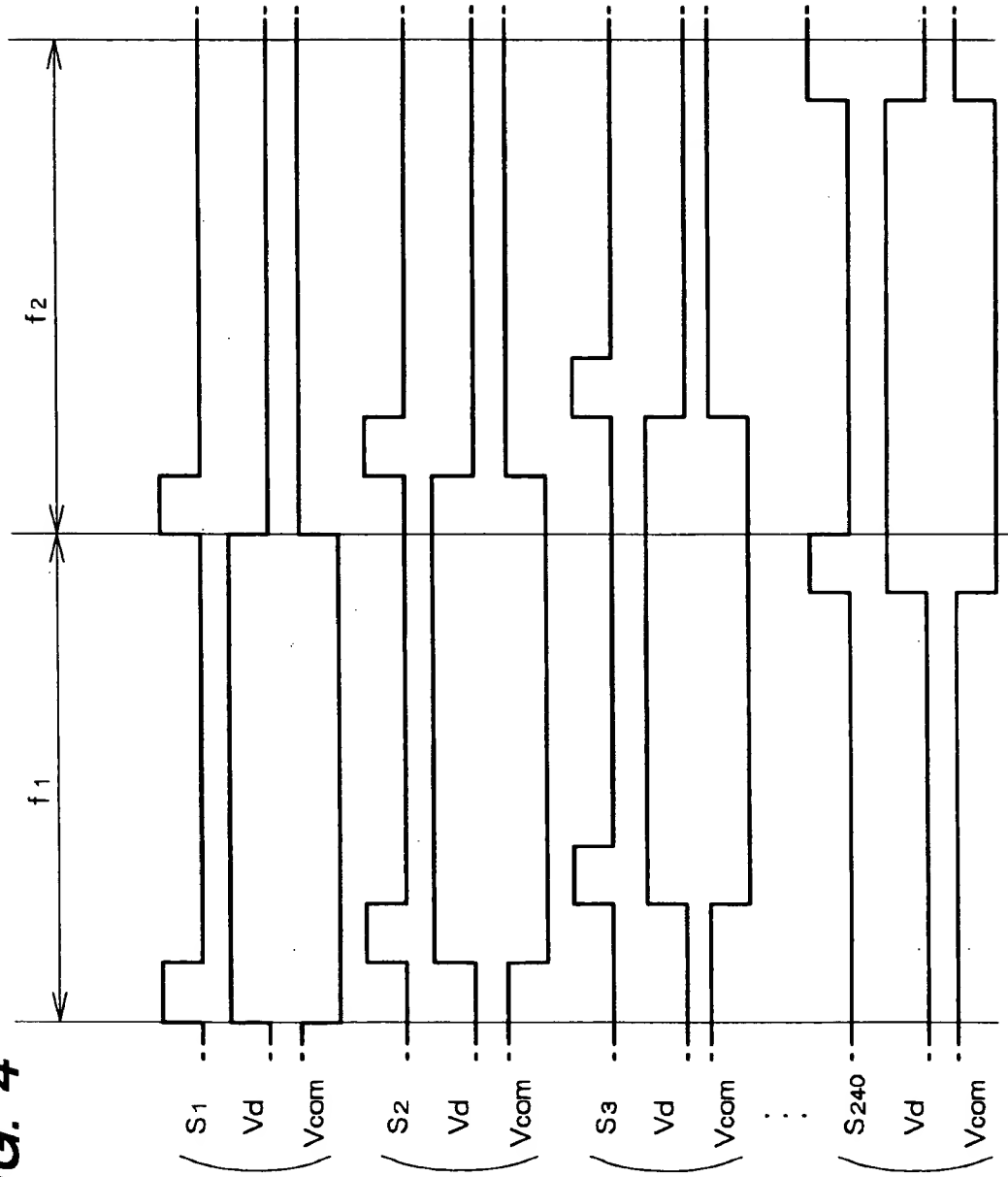
Time	FF1	FF2	FF3	FF4	FF5	...	FF240
$t$	0	0	0	0	0	...	0
$t+1$	1	0	0	0	0	...	0
$t+2$	1	1	0	0	0	...	0
$t+240$	1	1	1	1	1	...	1

Arrows indicate a progression from  $t$  to  $t+1$ ,  $t+1$  to  $t+2$ , and  $t+2$  to  $t+240$ . Each row is associated with a reference numeral 50, which points to the entire row of segments.

FIG. 3



**FIG. 4**



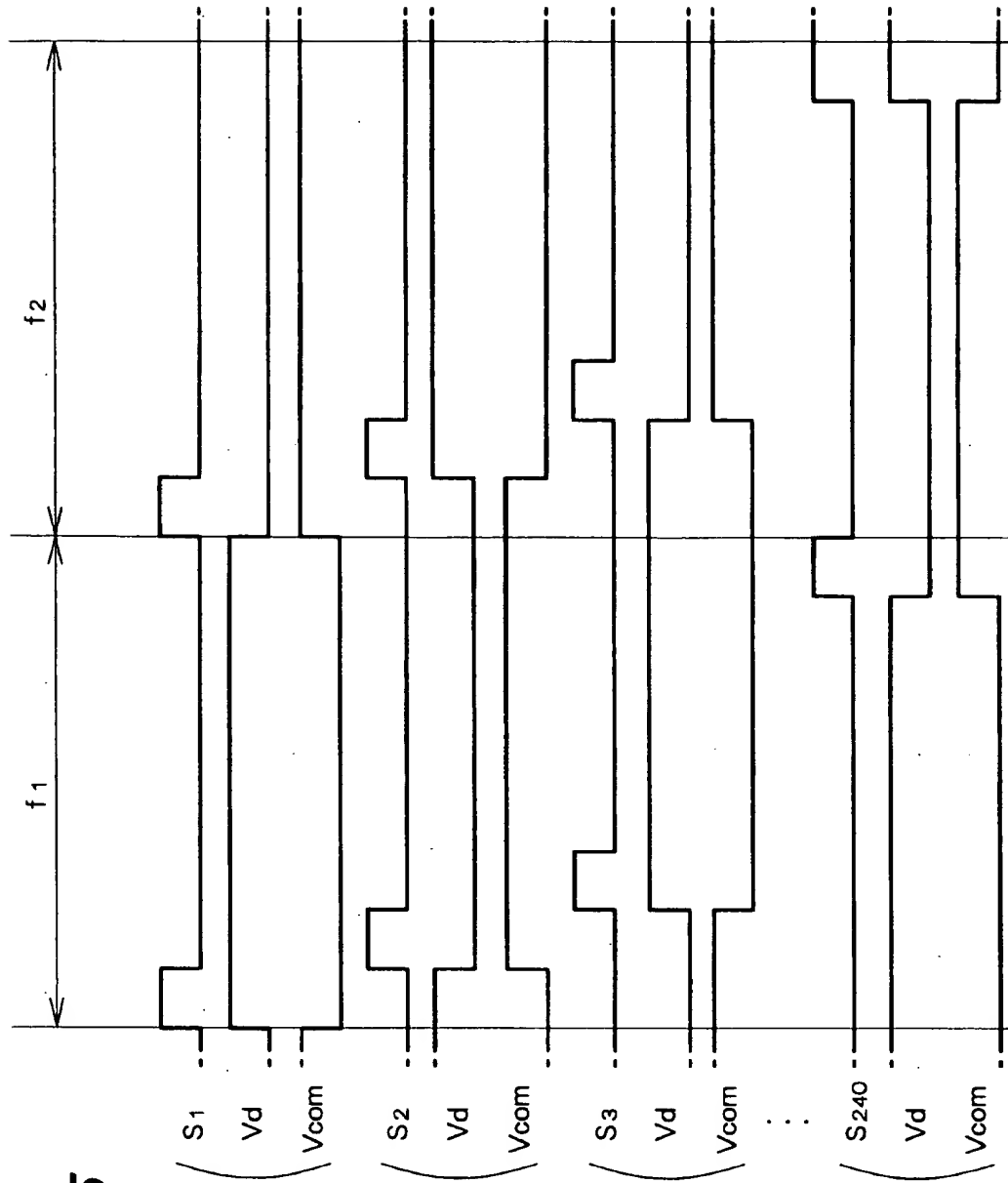
[illegible]

FIG. 6 is a block diagram of a semiconductor device. The device includes a data line driver circuit 10, a gate line driver circuit 120, a voltage divider circuit 114, a power supply circuit 116, and a crossbar array 30. The data line driver circuit 10 is connected to the gate line driver circuit 120 and the crossbar array 30. The gate line driver circuit 120 is connected to the crossbar array 30 and the voltage divider circuit 114. The voltage divider circuit 114 is connected to the power supply circuit 116. The crossbar array 30 includes a grid of access transistors (M11, M12, M21, M22, ..., Mmn) and storage capacitors (C1, C2, ..., Cn). The access transistors are controlled by gate signals (X1, X2, ..., Xn) and data signals (Y1, Y2, ..., Ym). The storage capacitors are connected to the access transistors and the data lines. The voltage divider circuit 114 provides a reference voltage to the gate line driver circuit 120. The power supply circuit 116 provides a power supply voltage to the gate line driver circuit 120.

FIG. 6

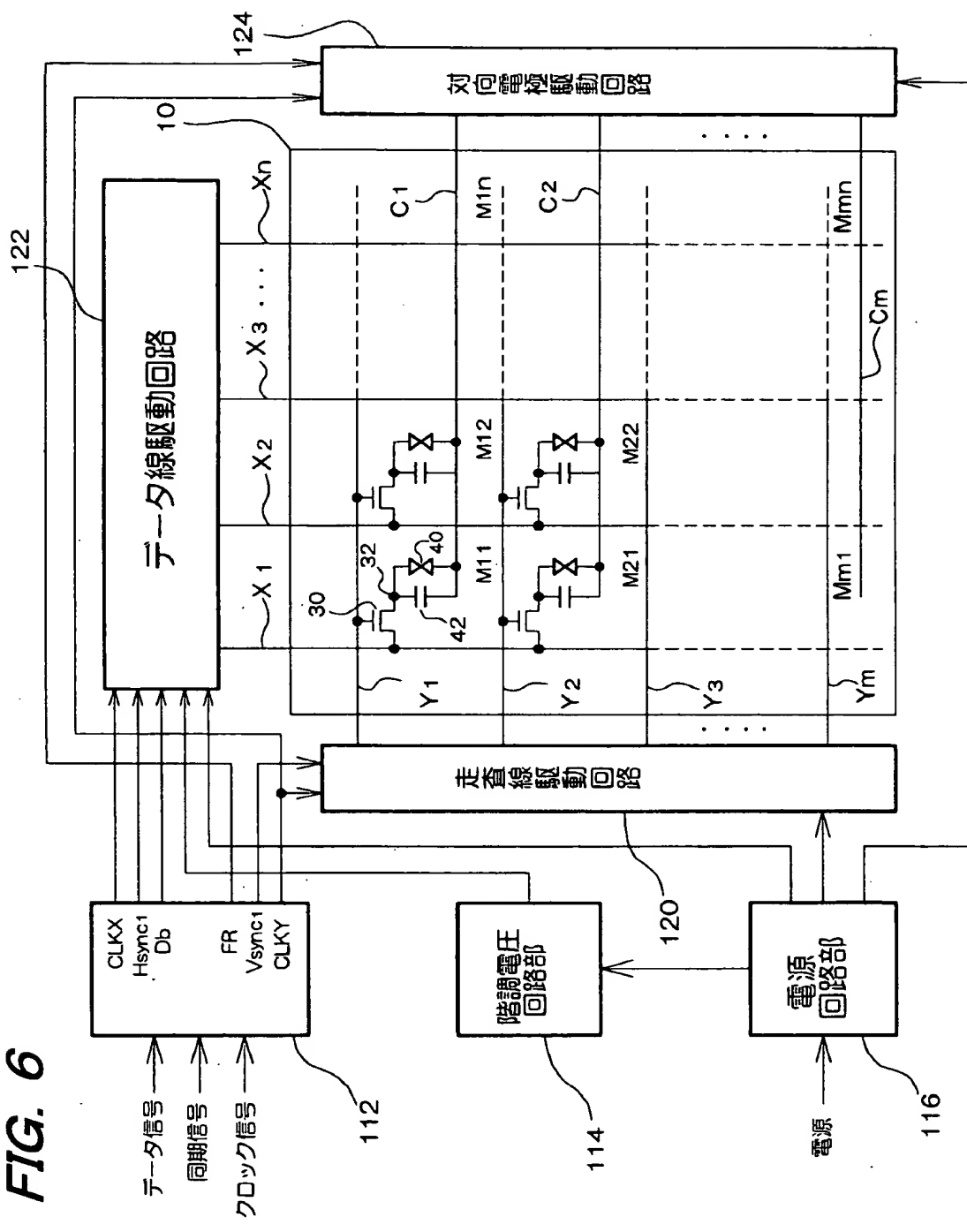
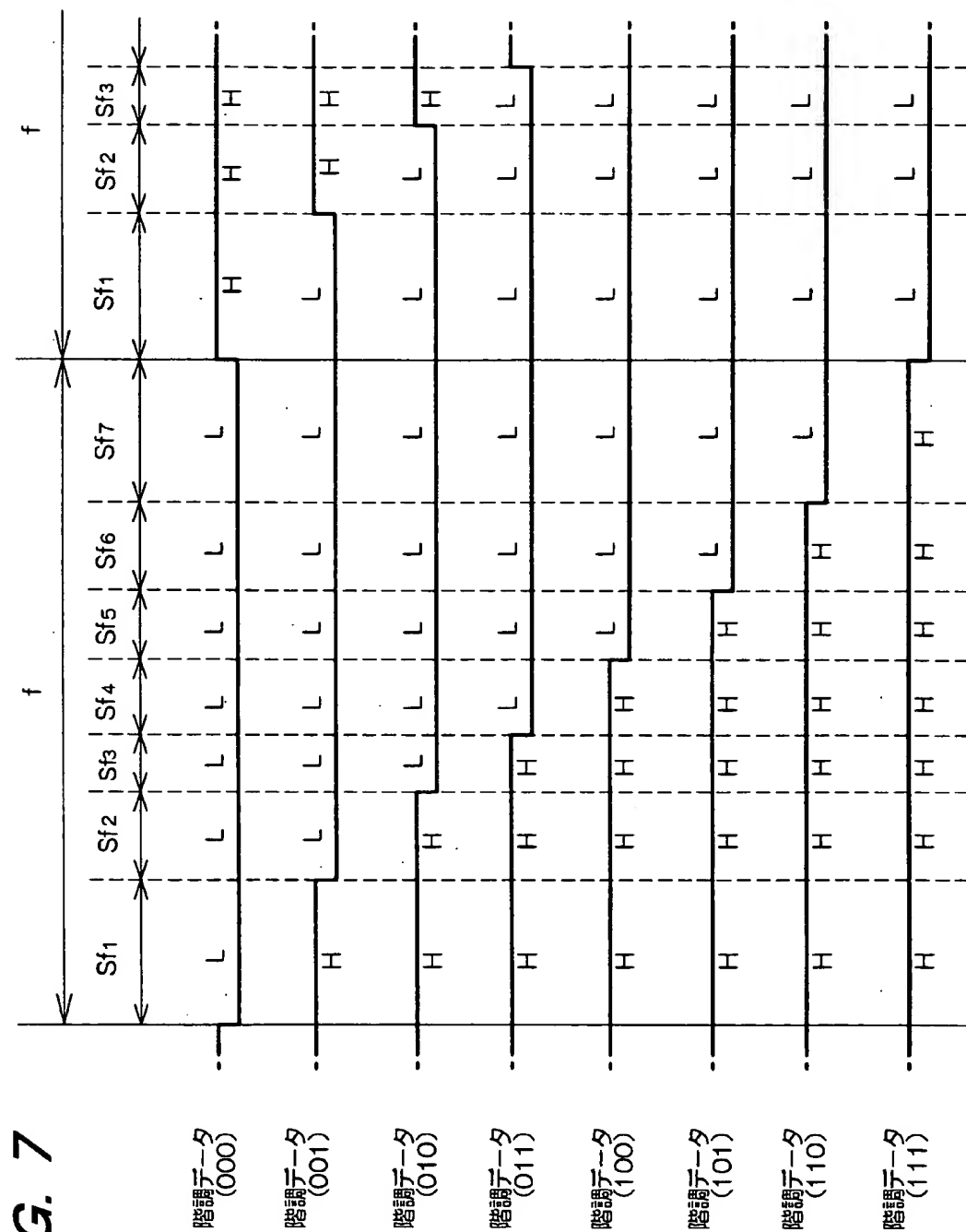
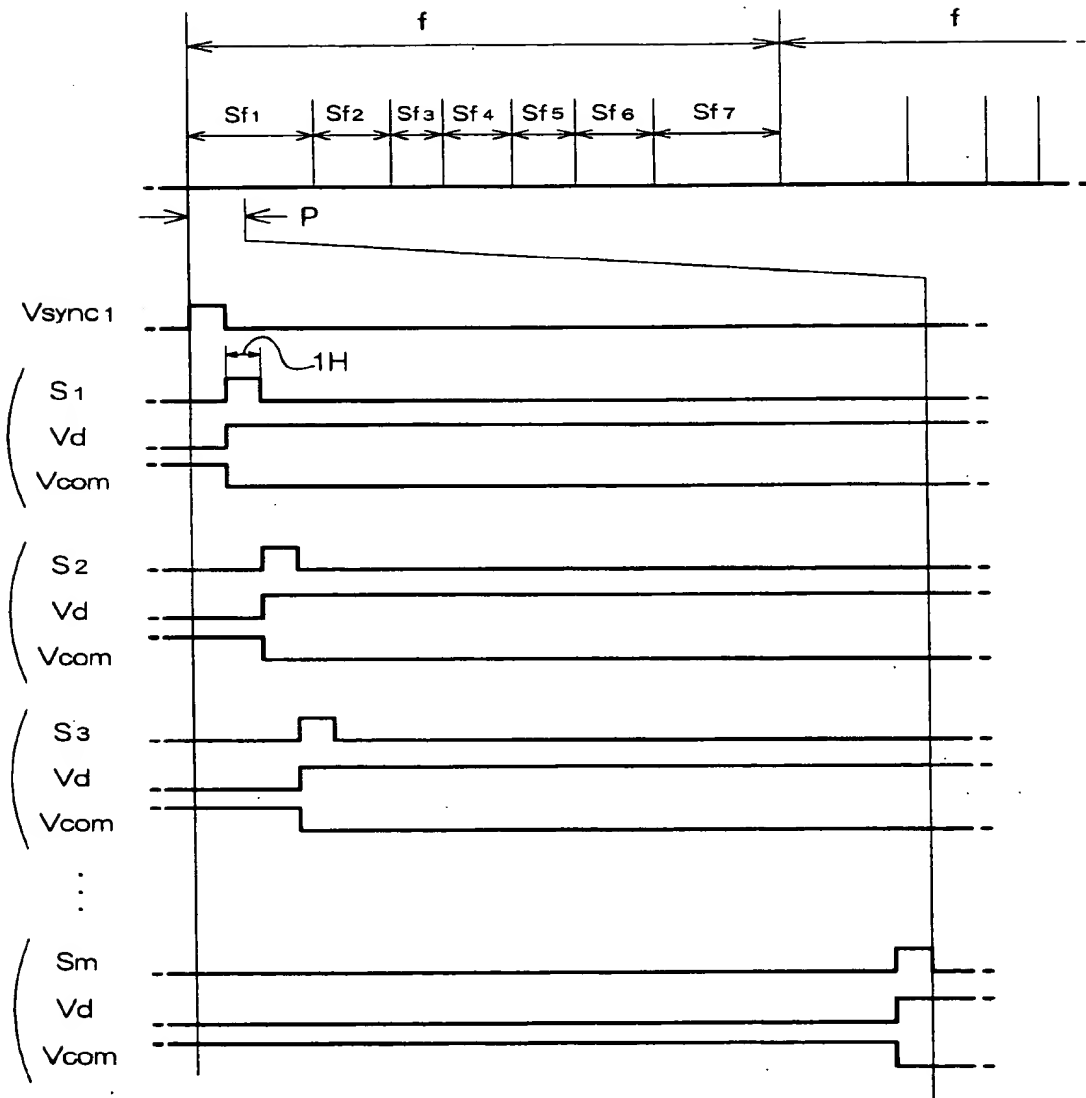


FIG. 7

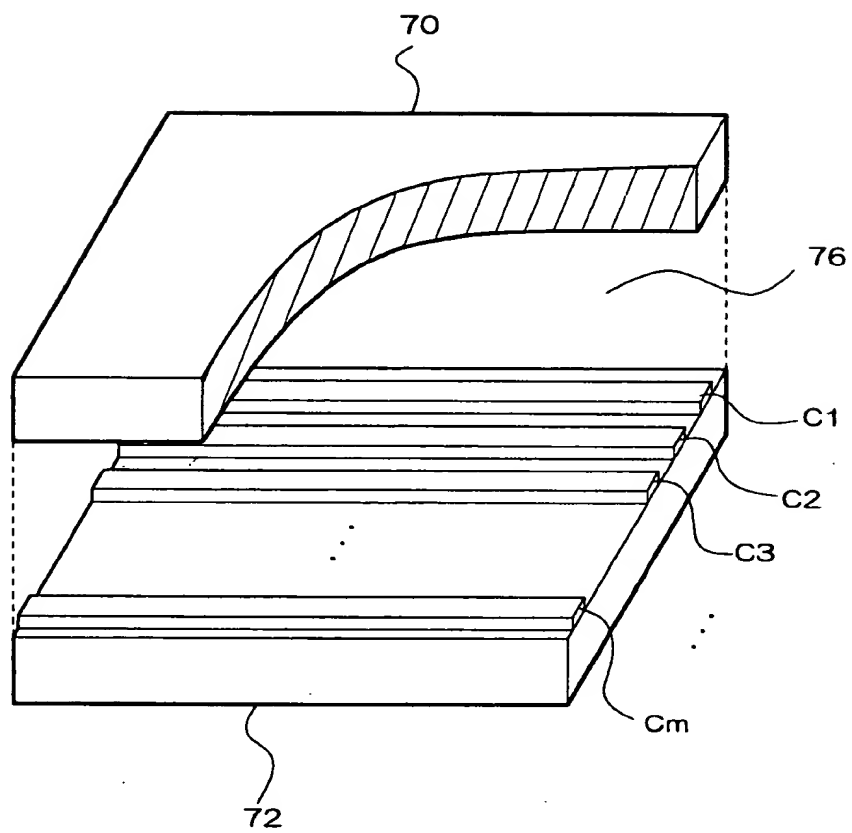


**FIG. 8**





**FIG. 9**



[illegible]対向電極の電圧  $V_{com}$ 

f1

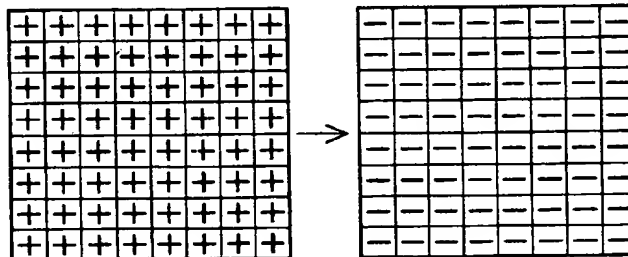
f2

**+V**

-v

f 1

f2



f 1

- f 2

[illegible]

FIG. 11A

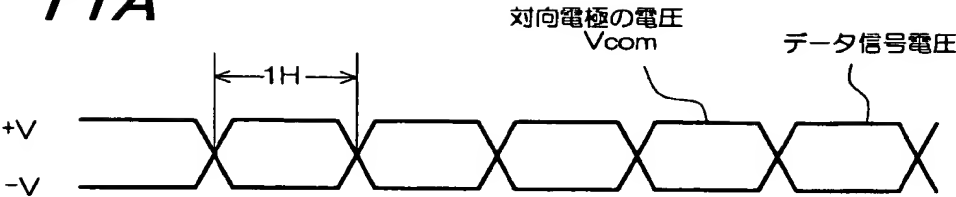


FIG. 11B

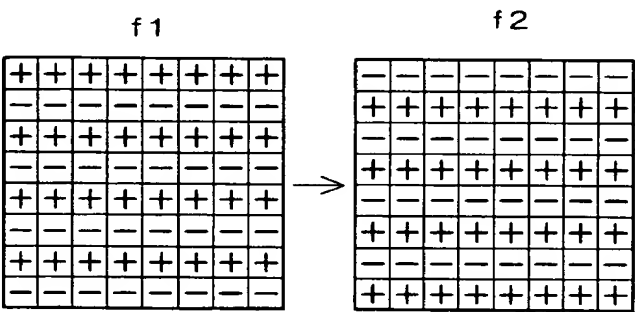
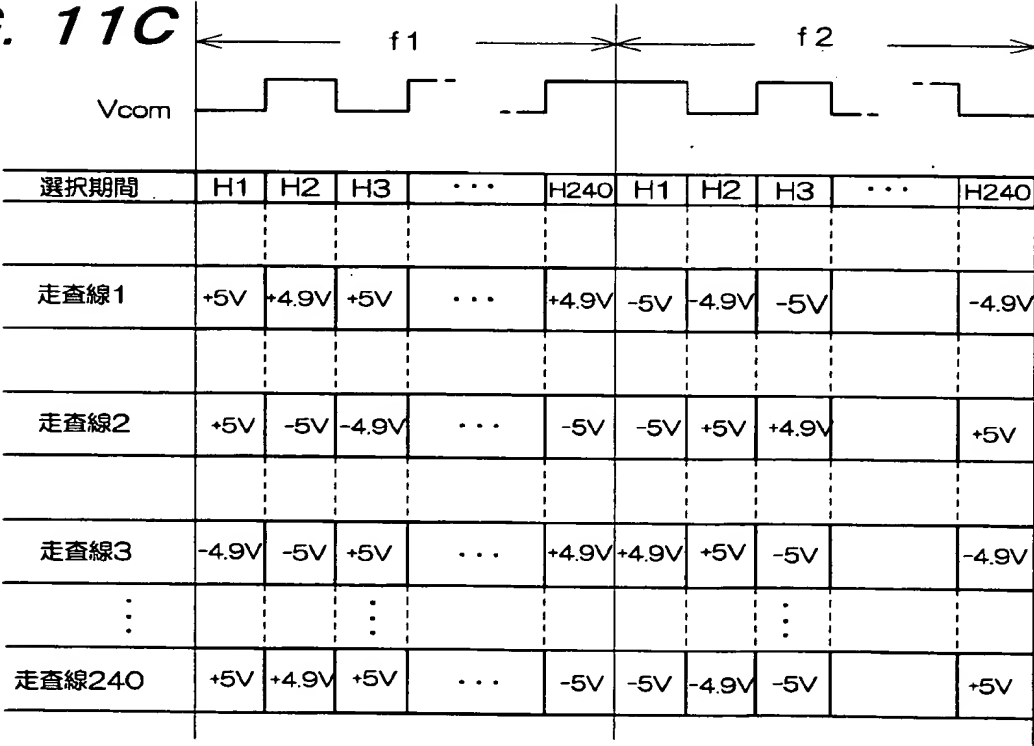


FIG. 11C



**FIG. 12**

